16. A method of applying instructions to a microprocessor during test mode, said method comprising:

a) entering a test mode establishing said microprocessor as a slave and a test controller as a master;

b) said test controller transferring to a queue an instruction to be executed in said microprocessor; and

c) said instruction causing at least one test instruction from a first memory to be executed by said microprocessor, said first memory comprising a plurality of test instructions.

17. The method of Claim 16 further comprising:

d) bypassing a second memory coupled to said microprocessor and forcing said microprocessor to execute instructions from said queue, said second memory comprising program instructions to be run when not in said test mode.

18. The method of Claim 16 further comprising:

d) entering a supervisory state in which instructions of said test instructions from said second memory are executed in said microprocessor.

19. The method of Claim 16 further comprising:

d) said microprocessor causing at least one test instruction from said second memory to be fed to said microprocessor in a supervisory state.

20. The method of Claim 19 further comprising:

e) writing to a register during said supervisory state, said register not writeable during said test mode when not in supervisory state.

21. The method of Claim 16 further comprising:

d) switching execution between instructions in said queue and said first memory, wherein said microprocessor switches between executing instructions originating from a test interface and said test instructions.